UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,446	10/29/2003	Arvind Kamath	03-1202/LSIIP233	7970

24319 7590 05/03/2005

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	10/697,446	KAMATH ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003 and 09 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *16-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-15* is/are rejected.

7)☒ Claim(s) *9-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 29 October 2003 and to applicant's election received on 09 March 2005.

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-15, in the reply received on 09 March 2005 is acknowledged. The traversal is on the grounds that the as-claimed inventions are not distinct because they both include the "implanting nitrogen" feature and also because the search of both inventions would not be burdensome.

Regarding the "implanting nitrogen" step, this is not found persuasive because it is a process limitation and claims 16-18 are directed to a system (i.e. a structure). The applicant is advised that, per MPEP section 2113, structure claims that include process limitations (i.e. product-by-process claims) are limited only to the structure implied by the steps (i.e. the structure implied by the process limitations). Accordingly, in determining the patentability of claims 16-18, it would not be adequate to search just for prior art structures that have implanted nitrogen. Instead, other prior art structures that are doped with nitrogen (e.g. those formed by a materially different process like

diffusing a nitrogen dopant as suggested in the restriction requirement mailed to the applicant on 17 February 2005) can also anticipate this limitation. In such cases, a prior art rejection can be made and the burden would be shifted to the applicant to show an unobvious difference.

Regarding the burden of searching both inventions, as indicated in the restriction requirement mailed to the applicant on 17 February 2005, the two inventions have acquired a separate status in the art as shown by their different classification, which would indeed make the search of both inventions burdensome.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 16-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of Forming an Antifuse on a Semiconductor Substrate that Includes Growing a Dielectric Oxide Layer on a Nitrided Substrate Portion by Wet Oxidation.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solo de Zaldivar (US 5,610,084) in view Soleimani et al. (US 5,330,920).

Referring to Figs. 1a-1d, 3, 4a-4c and column 2, line 51 to column 5, line 43, Solo de Zaldivar disclose a method of forming an antifuse that includes the following features:

- A silicon substrate (1) with field oxide regions (6) is provided;
- A lower antifuse electrode (4) is formed in the silicon substrate (1) by n-type implanting through an oxide layer (14) corresponding to an exposed antifuse region as shown in Fig. 4a;
- A mask (22) is used to implant nitrogen (23) through the oxide layer (14) corresponding to the exposed antifuse region as shown in Fig. 4b;
- The nitrogen ion implantation dose is approximately $4x10^{14}$ ions per cm^2;
- The oxide layer (14) is then removed by etching;

- A 5 nm (i.e. 50 angstroms) thick antifuse oxide layer (3) and a 10 nm thick tunnel oxide layer (18) are then simultaneously grown by thermal oxidation as shown in Fig. 3; and
- An upper antifuse electrode (5) is formed directly on the antifuse oxide (3).

These are limitations set forth in claims 1-2, 4, 6, 8 of the applicant's invention. Further regarding claim 6, the nitrogen implantation results in a thin silicon nitride layer (24) formed at the substrate surface with a thickness of approximately 1 nm (i.e. 10 angstroms) (see column 4, lines 1-3), which is well within the applicant's 200-600 angstroms limitation. Regarding claim 7, curve A in Fig. 2 indicates that antifuse oxides thinner than 5 nm down to about 2 nm (i.e. ranging from 20 to 50 angstroms) can be grown (also see column 3, lines 52-62).

However, Solo de Zaldivar does not expressly teach or suggest using wet oxidation for the thermal oxidation step, which is a limitation of claim 1. Also, Solo de Zaldivar does not expressly teach or suggest using wet oxidation at a temperature ranging from 800 to 900 degrees C, which is the further limitation to claim 1 set forth in claim 5 of the applicant's invention. Further, Solo de Zaldivar does not expressly teach or suggest a nitrogen implantation energy, which are further limitations to claim 1 set forth in claims 3-4 of the applicant's invention.

Regarding claims 1, 5, Soleimani et al. teach that an oxide layer can be grown on a nitrogen implanted silicon surface by wet oxidation at a temperature that ranges from 800 to 1000 degrees C (see column 3, lines 4-20). Regarding claims 3-4, Soleimani et

al. teach that nitrogen ions can be implanted using an energy that ranges from 10 to 50 KeV (see column 2, lines 48-56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Solo de Zalvidar and Soleimani et al. in order to grow the antifuse oxide layer of Solo de Zalvidar by wet oxidation as taught by Soleimani et al. and also to perform the nitrogen implanting step of Solo de Zalvidar using an energy that ranges from 10 to 50 KeV as taught by Soleimani et al. Soleimani et al. shows that thermal oxidation by wet or dry methods are recognized in the art as equivalent methods (see column 3, lines 6-10). Also, Soleimani et al. recognize that their energy range is suffiicient for implanting nitrogen through a sacrificial oxide layer but not through a resist mask (see column 2, lines 44-56) and Solo de Zaldivar use an oxide layer (14) with a mask (22) to implant nitrogen (23).

6. Claims 11, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solo de Zaldivar (US 5,610,084) in view Soleimani et al. (US 5,330,920) and Chiao et al. (US 4,757,359).

Referring to Figs. 1a-1d, 3, 4a-4c and column 2, line 51 to column 5, line 43, Solo de Zaldivar disclose a method of forming an antifuse that includes the following features:

- A silicon substrate (1) with field oxide regions (6) is provided;

- A lower antifuse electrode (4) is formed in the silicon substrate (1) by n-type implanting through an oxide layer (14) corresponding to an exposed antifuse region as shown in Fig. 4a;
- A mask (22) is used to implant nitrogen (23) through the oxide layer (14) corresponding to the exposed antifuse region as shown in Fig. 4b;
- A 5 nm (i.e. 50 angstroms) thick antifuse oxide layer (3) and a 10 nm thick tunnel oxide layer (18) are then simultaneously grown by thermal oxidation as shown in Fig. 3;
- An upper antifuse electrode (5) is formed directly on the antifuse oxide (3); and
- The antifuse is programmed by applying a voltage of approximately 8 volts between the lower electrode (4) and the upper electrode (5) (see column 3, lines 5-20).

These are limitations set forth in claims 11, 15 of the applicant's invention.

However, Solo de Zaldivar does not expressly teach or suggest using wet oxidation for the thermal oxidation step, which is a limitation of claim 11. Also, Solo de Zaldivar lacks the step of determining the programmed state of the antifuse, which is also a limitation of claim 11. Further, Solo de Zaldivar lacks the programming voltage being higher than the supply voltage feature of claim 15.

Soleimani et al. teach that an oxide layer can be grown on a nitrogen implanted silicon surface by wet oxidation (see column 3, lines 4-20). Chiao et al. teach that the programmed state of an oxide fuse can be read using a sense voltage of about 2 volts.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Solo de Zaldivar and Soleimani et al. in order to grow the antifuse oxide layer of Solo de Zaldivar by wet oxidation as taught by Soleimani et al. Soleimani et al. shows that thermal oxidation by wet or dry methods are recognized in the art as equivalent methods (see column 3, lines 6-10). It also would have been obvious to use a sense voltage as taught by Chiao et al. in order to determine if breakdown of the antifuse oxide layer of Solo de Zaldivar has occurred (i.e. to determine if the antifuse has been programmed).

7. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solo de Zaldivar (US 5,610,084), Soleimani et al. (US 5,330,920), and Chiao et al. (US 4,757,359) as applied to claim 11 above, and further in view of Fifield et al. (US 2004/0004269 A1).

As shown above the combination of Solo de Zaldivar, Soleimani et al., and Chiao et al. has all of the limitations set forth in claim 11 of the applicant's invention. However, this combination lacks the switchably coupled feature of claim 12, the transistor connected in series feature of claim 13, and the sense amplifier feature of claim 14. Referring to Fig. 6 and paragraphs [0039] to [0051], Fifield at al. teach an antifuse circuit that includes a current source (35) connected through a coupling transistor (36) to an antifuse element (200) and a transistor (31) for reading the antifuse (200) that is coupled to a voltage source (30) and a fuse latch (33). The read transistor (31) can operate as a switch or can be biased as an amplifier.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further combine the teachings of Solo de Zaldivar, Soleimani et al., and Chiao et al. with those of Fifield et al. in order to incorporate the antifuse circuit as taught by Fifield et al. Fifield et al. recognize that their antifuse circuit has the advantage of being able to read the programmed state of the antifuse independently from the actual antifuse programmed resistance (see paragraph [0051]).

Allowable Subject Matter

8. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if claim 9 were rewritten in independent form to include all of the limitations of claim 1.

9. The following is a statement of reasons for the indication of allowable subject matter: Claims 9-10 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming an antifuse on a semiconductor substrate that includes implanting nitrogen into a first portion of the substrate that corresponds to the antifuse combined with implanting nitrogen into a second portion of the substrate, wherein oxide layers are subsequently formed over both the first and second portions using the same wet oxidation step and the thickness of the oxide layers corresponding to the first and second portions are different.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chidambarrao et al. teach an antifuse fabricating method that features nitrogen implantation.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813